WHAT IS CLAIMED IS:

1. An address data processor for a plasma display panel (PDP), comprising:

a subfield data generator for receiving RGB video data, and generating corresponding subfield data;

a frame memory for storing the subfield data using a rising edge and a falling edge of a reference clock signal, and outputting the stored subfield data using the rising edge and the falling edge of the reference clock signal; and

a subfield data arranger for receiving the subfield data output by the frame memory, arranging the subfield data as address data for each subfield, and outputting the address data to represent gray on the PDP.

2. The processor of claim 1, wherein the subfield data is divided, and wherein the frame memory stores the divided subfield data using the rising edge and the falling edge of the reference clock signal, and outputs the stored divided subfield data using the rising edge and the falling edge of the reference clock signal.

3. The processor of claim 1, further comprising an RGB mixer for receiving the RGB video data, selecting data as a specific combination of the RGB video data, and outputting the selected data to the subfield data generator.

4. The processor of claim 3, wherein the specific combination includes two different color sets of video data selected from the RGB video data.

5. The processor of claim 4, wherein a selection order of the two different color sets of video data follows R → G → B and G → B → R, respectively.

6. The processor of claim 1, further comprising a subfield matrix for receiving the subfield data generated by the subfield data generator and output in series, converting the subfield data for a specific number of neighboring cells on the same line into parallel subfield data, and outputting the parallel subfield data to the frame memory.

7. The processor of claim 1, wherein the subfield data generator comprises a first subfield data generator and a second subfield data generator for respectively generating subfield data corresponding to two sets of video data selected from the RGB video data, and

the subfield matrix comprises a first subfield matrix and a second subfield matrix for respectively receiving the subfield data output in series by the first and second subfield data generators, generating parallel subfield data corresponding to a specific number of neighboring cells, and outputting the parallel subfield data.

8. The processor of claim 7, further comprising a concatenator for concatenating the parallel subfield data output by the first and second subfield matrices, and outputting the concatenated parallel subfield data to the frame

memory.

9. The processor of claim 1, further comprising a data buffer for receiving the subfield data generated by the subfield data generator, dividing the subfield data into two subfield data sets, providing the two subfield data sets to the frame memory using the rising edge and the falling edge of the reference clock signal, respectively, reading the subfield data sets using the rising edge and the falling edge, respectively, of the reference clock signal, and providing the two subfield data sets to the subfield data arranger.

10. The processor of claim 9, wherein the frame memory comprises a first frame memory and a second frame memory, and wherein a first subfield data set of the two subfield data sets is stored in the first frame memory and a second subfield data set of the two subfield data sets is stored in the second frame memory.

11. The processor of claim 10, wherein the data buffer provides the first subfield data set to the first frame memory responsive to the rising edge of the reference clock signal, and provides the second subfield data set to the second frame memory responsive to the falling edge of the reference clock signal.

12. The processor of claim 10, wherein the data buffer reads the first subfield data set from the first frame memory responsive to the rising edge

of the reference clock signal, and reads the second subfield data set from the second frame memory responsive to the falling edge of the reference clock signal.

13. A method for processing address data in a plasma display panel (PDP), comprising:

(a) generating subfield data corresponding to RGB input video data;

(b) storing the subfield data in a frame memory using a rising edge and a falling edge of a reference clock signal;

(c) reading the subfield data stored in the frame memory using the rising edge and the falling edge of the reference clock signal; and

(d) arranging the subfield data read from the frame memory as address data for each subfield, and outputting the address data to the PDP to represent gray on the PDP.

14. The method of claim 13, further comprising dividing the subfield data between (a) and (b), wherein (b) comprises storing the divided subfield data in the frame memory using the rising edge and the falling edge of the reference clock signal, and (c) comprises reading the divided subfield data stored in the frame memory using the rising edge and the falling edge of the reference clock signal.

15. The method of claim 13, wherein (a) comprises:

selecting video data as a specific combination of the RGB input video

data; and

generating the subfield data corresponding to the selected video data.

16. The method of claim 15, wherein the specific combination includes two different color sets of video data selected from the RGB video data.

17. The method of claim 16, wherein the a selection order of the two different color sets of video data follows R → G → B and G → B → R, respectively.

18. The method of claim 13, wherein the subfield data generated in (a) are output in series, and

the method further comprises, between (a) and (b),

(e) receiving the subfield data output in series;

(f) converting the subfield data for a specific number of neighboring cells on the same line into parallel subfield data; and

(g) outputting the parallel subfield data to the frame memory.

19. The method of claim 18, wherein (a) comprises generating first subfield data corresponding to a first of two sets of video data selected from the RGB video data, and generating second subfield data corresponding to a second of the two set of video data, and outputting each of the first and second subfield data in series,

(e) comprises receiving the first and second subfield data output in

series,

(f) comprises generating first parallel subfield data using the first subfield data and generating second parallel subfield data using the second subfield data, and

(g) comprises outputting the first and second parallel subfield data.

20. The method of claim 19, further comprising, after (g), concatenating the first and second parallel subfield data into a single parallel subfield data, and providing the concatenated parallel subfield data to the frame memory.

21. The method of claim 20, wherein the frame memory comprises a first frame memory and a second frame memory, the method further comprising dividing the concatenated parallel subfield data into first subfield data set and a second subfield data set.

22. The method of claim 21, further comprising storing the first subfield data set in the first frame memory responsive to the rising edge of the reference clock signal, and storing the second subfield data set in the second frame memory responsive to the falling edge of the reference clock signal.

23. The method of claim 21, further comprising reading the first subfield data set from the first frame memory responsive to the rising edge of the reference clock signal, and reading the second subfield data set from the second frame memory responsive to the falling edge of the reference clock

signal.

24. In a method for processing address data in a plasma display panel (PDP), a recording medium for storing a program for performing address data processing operations comprising:

(a) generating subfield data corresponding to RGB input video data;

(b) storing the subfield data in a frame memory using a rising edge and a falling edge of a reference clock signal;

(c) reading the subfield data stored in the frame memory using the rising edge and the falling edge of the reference clock signal; and

(d) arranging the subfield data read from the frame memory as address data for each subfield, and outputting the address data to the PDP to represent gray on the PDP.

25. An address data processor for a plasma display panel (PDP), comprising:

a subfield data generator for receiving video data having at least one color, and generating corresponding subfield data;

a frame memory for storing the subfield data using a rising edge and a falling edge of a reference clock signal, and outputting the stored subfield data using the rising edge and the falling edge of the reference clock signal; and

a subfield data arranger for receiving the subfield data output by the frame memory, arranging the subfield data as address data for each subfield, and outputting the address data to represent gray on the PDP.

26. The processor of claim 25, wherein the subfield data is divided, and wherein the frame memory stores the divided subfield data using the rising edge and the falling edge of the reference clock signal, and outputs the stored divided subfield data using the rising edge and the falling edge of the reference clock signal.

27. The processor of claim 25, further comprising a subfield matrix for receiving the subfield data generated by the subfield data generator and output in series, converting the subfield data for a specific number of neighboring cells on the same line into parallel subfield data, and outputting the parallel subfield data to the frame memory.

28. The processor of claim 25, further comprising a data buffer for receiving the subfield data generated by the subfield data generator, dividing the subfield data into two subfield data sets, providing the two subfield data sets to the frame memory using the rising edge and the falling edge of the reference clock signal, respectively, reading the subfield data sets using the rising edge and the falling edge, respectively, of the reference clock signal, and providing the two subfield data sets to the subfield data arranger.